TRBv3 - FPGA based, universal readout board for physics experiments

Grzegorz Korcyl
Plan

1. Data Acquisition Systems
2. TDC Readout Board v2
3. Trigger Readout Board v3
4. FPGA based TDCs
5. Addon system
6. Networking
7. Projects
8. Summary
Data Acquisition Systems

- Electronics and software that allows to measure and collect data from detectors

Real experiment:
- Different detector types
- Thousands of data channels
- Thousands of measurements per second
- On fly data analysis
Programmable Electronics

- **Detectors**: 
  - Continuously generate analog signals
  - Thousands of channels

- **Front-End Electronics**: 
  - Analog signal shaping
  - Discrimination

- **Readout electronics**: 
  - Measurement and digitalization of analog signals
  - Preliminary analysis
  - Data units construction

- **Concentrators**: 
  - Assembly of data units
  - Gateway to the network
  - Transmission of control data

- **Trigger module**: 
  - Generates a “snapshot” signal
  - Controls the operation of the system

- **Event Builder**: 
  - Combines data units into entire events
  - Stores data on permanent storage device
Field Programmable Gate Arrays

- Programmable logic device
- Reconfigurable by the user
- Parallel processing
- Real-time processing
- Hardware features:
  - Memory blocks
  - Communication ports
  - Digital Signal Processing units
  - CPU solutions
  - CPU solutions
TDC Readout Board v2

- 4x HPTDC
  - 32 channels each
  - Up to 17ps resolution

- 1x Xilinx Virtex4 FPGA
  - TDC readout control

- 1x ETRAX
  - Interface for slow control

- 1x 2,5Gbps Optical link
  - Data output
  - Connection to the larger system

- 1x Sharc DSP

- 1x RJ45
  - Interface to network

- 1x Addon connector
  - Extension board slot

- 1x Reference time input
Trigger Readout Board v3

- 5x Lattice ECP3 150 FPGAs
  - 4 edge devices
  - 1 central
  - Flash ROMs for each

- 8x 3.2GBps optical links

- 4x 208pin QMS connectors
  - Small Addons

- 1x 106pin connector
  - Large Addon
FPGA based TDCs
FPGA based TDCs - Carry Chain

- Delays - multiplexers between bins
FPGA based TDCs – Bin width

- Arrays/block boundaries – „Ultra Wide Bins”
- Sensitive to temperature and voltage variations
- Values vary between 3 ps – 100 ps
- PAR constraints very important

![Graph showing bin width distribution and RMS vs temperature and voltage]
FPGA based TDCs - Calibration

- LookUp Table with delays for each bin

- Ideas:
  1. Double registration
     - Delay line long as the input signal period
     - Catches two signal edges (bins B1, B2) with known time difference
     - Bin delay calculated as \( T_b = \frac{T_p}{(B2 - B1)} \)
     - Fast, easy but less accurate (UWB)
  2. Statistical approach
     - Inject M signals not correlated with TDC clock
     - Count hits on each bin (N)
     - Calculate bin width as \( T_b = \frac{N \times T_p}{M} \)
     - Complex, resource consuming but accurate results
FPGA based TDCs - Wave Union

- Carry chain stores a pattern of 0-1 and 1-0 transitions
- Pattern is released when signal arrives
- Improvement to range 1 ps – 40 ps /bin
FPGA based TDCs - Performance

- RMS ~9ps
- Deadtime for 2 clock cycles

Table 7: Effective HPTDC resolution based on cable delay measurements

<table>
<thead>
<tr>
<th>Mode</th>
<th>Resolution (RMS)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Low resolution</td>
<td>0.34 bin (265 ps)</td>
</tr>
<tr>
<td>Medium resolution</td>
<td>0.44 bin (86ps)</td>
</tr>
<tr>
<td>High resolution</td>
<td>0.65 bin (64ps)</td>
</tr>
<tr>
<td>High resolution DLL tap adjust INL table correction</td>
<td>0.35 bin (34ps)</td>
</tr>
<tr>
<td>Very high resolution</td>
<td>2.4 bin (58ps)</td>
</tr>
<tr>
<td>Very high resolution DLL tap adjust INL table correction</td>
<td>0.72 bin (17 ps)</td>
</tr>
</tbody>
</table>
Addon System

- 4x 208 pin connectors
- 1x 106 pin connector

Features:
- Data transfer
- 3,3V and 6V power supply

Addon boards
- Input signal converters
- Front-end modules
- Additional measurement devices
- Input / output extensions

Applications:
- Measurement
- Trigger module
- Network hub
Networking

- TRBv3 designed to be used as
  - Stand-alone measurement device
  - Part of a complex system

- Different communication solutions
  - Based on 3.2GBps optical links
  - Managed by central FPGA
  - Transmission of collected data
  - Control of the board
Networking

- Board management
  - Gigabit Ethernet link
    - Full Duplex
    - Basic protocols (IP, UDP, ARP, DHCP, ICMP, Custom)
    - Autonegotiation + network address acquisition
Projects

- **Time measurement**
  - Straw Tube Tracker for PANDA (Jagiellonian University)
    - Drift time
    - Time over Threshold
  - Barrel DIRC and Disc DIRC for PANDA (GSI, JLU)

- Scintillator based PET (Jagiellonian University)
  - Time difference between modules

- Replacement of TRB2 in HADES (GSI)
Projects

- Charge measurement
  - RPC based PET project (LIP)

- Electromagnetic Calorimeter for HADES (UJ, GSI)

- Others
  - Detector readout for CBM (GSI)
  - Networking projects (UJ)
Summary

- TRBv3 as a versatile solution for readout of different kind of detectors
- Extensible thanks to system of addon boards
- Flexible integration with DAQ systems thanks to communication features

Advanced project:
- Hardware developed
- Ongoing work on software

Already planned to be used in many upcoming experiments